

WHAT IS CLAIMED IS:

1. A receiver circuit for receiving a receive signal that undergoes a given number or more transitions in a given time, comprising:

a processing unit for processing said receive signal; and

5 a signal detection unit that accepts said receive signal, includes a transition number detection circuit for detecting a number of transitions of a signal obtained based on said receive signal and outputs a signal for controlling an operation of said processing unit when said number of transitions detected by said transition number detection circuit is not more than a set value.

10 2. A receiver circuit for receiving a receive signal that undergoes a given number or more transitions in a given time, comprising:

a processing unit for processing said receive signal; and

a signal detection unit that accepts said receive signal, includes an amplitude detection circuit for detecting amplitude of said receive signal and outputs a signal for
15 controlling an operation of said processing unit when said amplitude detected by said amplitude detection circuit is not more than a set value.

3. The receiver circuit of Claim 1,
wherein said receive signal is a data signal or a clock signal.

4. The receiver circuit of Claim 2,
20 wherein said receive signal is a data signal or a clock signal.

5. The receiver circuit of Claim 1,
wherein said receive signal is a data signal and a clock signal received through a cable in which a plurality of transfer paths are integrated, and one of said data signal and said clock signal is input to said signal detection unit.

25 6. The receiver circuit of Claim 2,

wherein said receive signal is a data signal and a clock signal received through a cable in which a plurality of transfer paths are integrated, and one of said data signal and said clock signal is input to said signal detection unit.

7. The receiver circuit of Claim 2,

5 wherein said amplitude detection circuit includes an offset buffer that accepts said receive signal and outputs a HIGH or LOW signal when said amplitude of said receive signal is not more than a set value.

8. The receiver circuit of Claim 7,

10 wherein said signal detection unit includes a set value change circuit for changing said set value of said offset buffer.

9. The receiver circuit of Claim 8,

wherein said set value is changed by said set value change circuit on the basis of data stored in an externally readable and writable resistor.

10. The receiver circuit of Claim 1,

15 further comprising an offset buffer that accepts said receive signal and outputs a HIGH or LOW signal when amplitude of said receive signal is not more than a set value,

wherein said HIGH or LOW signal output by said offset buffer is input to said transition number detection circuit as said signal obtained based on said receive signal.

11. The receiver circuit of Claim 1,

20 wherein said processing unit is a data processing unit for processing a data signal received as said receive signal and is reset in accordance with said signal output by said signal detection unit.

12. The receiver circuit of Claim 2,

25 wherein said processing unit is a data processing unit for processing a data signal received as said receive signal and is reset in accordance with said signal output by said

signal detection unit.

13. The receiver circuit of Claim 1,

wherein said processing unit is a data processing unit for processing a data signal received as said receive signal and is power-down operated in accordance with said signal
5 output by said signal detection unit.

14. The receiver circuit of Claim 2,

wherein said processing unit is a data processing unit for processing a data signal received as said receive signal and is power-down operated in accordance with said signal
output by said signal detection unit.

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